Floating millivolt reference for PTAT current generation in Subthreshold MOS LSIs

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Abstract—A floating millivolt reference circuit to generate a PTAT current was developed by using MOSFETs operated in the subthreshold region. The circuit generates a floating voltage of about 10 mV. The variations in the reference are ±2.7 % in a temperature range from −20 to 100 °C. The accuracy of the reference circuit can be improved to ±0.3 % with a correction technique using a curvature-correction circuit. The total power consumption of the circuit was 4.6 μW at 100 °C.

I. INTRODUCTION

Intelligent-network systems with various smart-sensor devices are expected to be developed that will spread all over the world to enable infrastructures to be constructed for the information age. Such network systems will require a huge number of sensor LSIs that measure various physical data from our surroundings, store and process these measured data, and output them on demand. As these sensors must operate for long periods of time, the available energy resources—whether small batteries, energy harvesting, or both—limit their overall operation. One possible method of minimizing the energy they consume is to design a circuit in the subthreshold region of MOSFETs.

The sensing of temperature by these LSIs is one of their most fundamental applications. A sensory signal that is proportional to absolute temperature (PTAT) is necessary to construct a temperature sensor. However, as the subthreshold current of MOSFETs is an exponential function of the gate-source voltage, the PTAT current cannot be generated easily. In this paper, we propose a floating millivolt reference circuit that can be used to generate PTAT current in circuits [1]. In the following, Section II describes the method of generating PTAT current for the temperature sensor, Section III presents the floating millivolt reference with the results of SPICE simulation, and Section IV describes the curvature-correction techniques to obtain a high-accuracy reference.

II. GENERATION OF PTAT CURRENT

The subthreshold current \( I_D \) of a MOSFET is an exponential function of gate-source voltage \( V_{GS} \) and is given by

\[
I_D = I_0 \exp \left( \frac{V_{GS} - V_{TH}}{\eta V_T} \right),
\]

where \( I_0 \) is a process-dependent parameter, \( \eta \) is the subthreshold slope factor, and \( V_T = k_B T / e \) is the thermal voltage [2]. Assume that two MOSFETs are biased with two different voltages \( V_{GS1} \) and \( V_{GS2} \) to generate two subthreshold currents \( I_{D1} \) and \( I_{D2} \). The difference in the current ratios is given by

\[
\frac{I_{D2}}{I_{D1}} - \frac{I_{D1}}{I_{D2}} = \exp \left( \frac{V_{GS2} - V_{GS1}}{\eta V_T} \right) - \exp \left( \frac{V_{GS1} - V_{GS2}}{\eta V_T} \right).
\]

Equation (2) can be rewritten for a voltage difference of \( |V_{GS2} - V_{GS1}| < \eta V_T \)

\[
\frac{I_{D2}}{I_{D1}} - \frac{I_{D1}}{I_{D2}} = \frac{V_{GS2} - V_{GS1}}{\eta V_T}.
\]

The reciprocal of Eq. (3) is expressed as

\[
\frac{I_{D1}}{I_{D2}} - \frac{I_{D2}}{I_{D1}} = \frac{\eta V_T}{2(V_{GS2} - V_{GS1})} = \frac{\eta k_B}{2e(V_{GS2} - V_{GS1}) T}.
\]

The PTAT characteristic can be obtained for a fixed temperature-independent voltage difference of \( |V_{GS2} - V_{GS1}| \).

In practical circuit implementation, the division and the subtraction of the currents can be performed by translinear circuit and current mirror circuit [1]. However, generating a small temperature-independent floating reference voltage (≈ 10 mV) to generate the PTAT signal in Eq. (4) is not easy using a MOSFET operated in the subthreshold region. In the following sections, we develop a floating millivolt reference circuit.

III. FLOATING REFERENCE CIRCUIT

A. Circuit Configuration

A bandgap reference circuits are widely used to obtain a constant reference voltage and a floating reference voltage [3]. However, they are not suitable for our purpose because they need large resistors with high resistance for low-current operation in the subthreshold region. Buck and others proposed a new CMOS bandgap reference circuit without the use of resistors [4]. We modified their circuit to operate in the subthreshold region and to generate a floating millivolt reference.

Figure 1 shows the circuit configuration. The circuit consists of two diode-connected transistors \( (M_{D1}, M_{D2}) \) and two differential pairs \( (M_1, M_2, M_3, M_4) \). We set the aspect ratios \( K \) of these transistors such that

\[
K_{D1} > K_{D2}, \ K_1 < K_2, \text{ and } K_3 > K_4.
\]
The circuit generates output voltages on output terminals \( V_{\text{out}1}, V_{\text{out}2} \), and the difference in the voltages is the floating millivolt reference voltage. The floating reference voltage is equal to the sum of the differences in threshold voltage for different transistor size. The threshold voltage of a transistor depends on the length and width of its channels [5]. Therefore, the difference in threshold voltage can be used to generate a floating millivolt reference voltage. Output voltages \( V_{\text{out}1} \) and \( V_{\text{out}2} \) have a negative dependence on temperature, whereas the difference in the voltage of \( V_{\text{out}2} - V_{\text{out}1} \) shows a temperature-insensitive constant reference voltage. The details on the circuit operation are as follows.

The diode-connected MOSFETs \( M_{D1} \) and \( M_{D2} \) are operated in the subthreshold region, and their gate-source voltages \( V_{GS,D1} \) and \( V_{GS,D2} \) are given by

\[
V_{GS,Di} = V_{TH,Di} + \eta V_T \ln \left( \frac{I_{\text{bias}}}{K_i I_0} \right) \quad (i = 1, 2).
\]  

The difference in the gate-source voltages \( \Delta V_{GS,D} \) in \( M_{D1} \) and \( M_{D2} \) can be expressed as

\[
\Delta V_{GS,D} = \Delta V_{TH,D1} + \eta V_T \ln \left( \frac{K_{D1}}{K_{D2}} \right),
\]  

where \( \Delta V_{TH,D1} \) is the difference in the threshold voltages. The resulting currents \( I_1 \) and \( I_2 \) in differential pair \( M_1-M_2 \) are given by

\[
I_i = K_i I_0 \exp \left( \frac{V_i - V_{GS,Di} - V_{THi}}{\eta V_T} \right) \quad (i = 1, 2),
\]  

where \( V_i \) is the common-source node voltage of the differential pair. Current \( I_2 \) is copied into the \( M_4 \) of the differential pair \( M_3-M_4 \). Because the currents in transistors \( M_3 \) and \( M_4 \) are \( I_1 \) and \( I_2 \), gate-source voltages \( V_{GS,3} \) and \( V_{GS,4} \) are given by

\[
V_{GS,i+2} = V_{TH,i+2} + \eta V_T \ln \left( \frac{I_i}{K_i I_0} \right) \quad (i = 1, 2).
\]  

The difference \( \Delta V_{REF} = V_{out2} - V_{out1} \) in the output voltages is given by

\[
\Delta V_{REF} = V_{GS,4} - V_{GS,3}.
\]  

Equation (10) can be rewritten from Eqs. (7), (8), and (9) as

\[
\Delta V_{REF} = \Delta V_{TH,43} + \Delta V_{TH,12} - \Delta V_{TH,D21} + \eta V_T \ln \left( \frac{K_3 K_2 K_{D2}}{K_4 K_1 K_{D1}} \right),
\]  

where \( \Delta V_{TH,43} \) and \( \Delta V_{TH,12} \) are the differences in the threshold voltages. We set the aspect ratios \( K \), with condition of Eq.(5), such that

\[
K_3 K_2 K_{D2} = K_4 K_1 K_{D1}.
\]  

Then, the difference in voltage is constant with temperature. The floating voltage reference of the circuit is given by

\[
\Delta V_{REF} = \Delta V_{TH,43} + \Delta V_{TH,12} - \Delta V_{TH,D21}.
\]  

We can obtain the floating millivolt reference by adjusting the size of the transistors.

B. Simulation Results

We confirmed the operation of the circuit by SPICE simulation, assuming a set of 0.35-μm 2P4M-standard CMOS parameters and a 1.5-V power supply.

Figure 2 shows simulated output voltages of \( V_{out1} \) and \( V_{out2} \) as a function of temperature from -20 to 100 °C. Both the output voltages decrease linearly with temperature and maintain a constant difference in voltage. Figure 3 shows the floating reference voltage \( \Delta V_{REF} \). The difference is
almost constant and was about 10 mV. However, the floating reference voltage increases at low- and high-temperatures, and has nonlinear characteristics due to nonlinearity of the diode-connected transistors. The variations in the reference voltage were about ± 2.7 %. This nonlinearity degenerates the precision with which the PTAT current is generated.

IV. CURVATURE-CORRECTION TECHNIQUES

We develop curvature-correction techniques to improve the accuracy of the floating reference voltage. Several curvature-correction techniques have been presented in the literature [6]-[9]. We use an idea based on the piecewise-linear curvature-correction technique [9]. The details on circuit operation are as follows.

A. Curvature-Correction Architecture

The correction is performed by changing the bias current in diode-connected transistor M_{D2}. The bias current in diode-connected transistor M_{D2} is increased at low- and high-temperatures by using curvature-correcting current \( I_{\text{curv}} \).

The gate-source voltage \( V_{GS,D2} \) of transistor M_{D2} is now given by

\[
V_{GS,D2} = V_{TH,D2} + \eta V_T \ln \left( \frac{I_{\text{bias}} + I_{\text{curv}}}{K_{D2} I_0} \right).
\]  (14)

The difference \( \Delta V_{GS,D} \) in the gate-source voltages in M_{D1} and M_{D2} can be expressed as

\[
\Delta V_{GS,D} = \Delta V_{TH,D2} + \eta V_T \ln \left( \frac{K_{D1} (I_{\text{bias}} + I_{\text{curv}})}{K_{D2} I_{\text{bias}}} \right). \]  (15)

The difference in the output voltage \( \Delta V_{\text{REF}} \) can be given by

\[
\Delta V_{\text{REF}} = \Delta V_{TH} + \Delta V_{TH,D1} - \Delta V_{TH,D2} + \eta V_T \ln \left( \frac{I_{\text{bias}}}{I_{\text{bias}} + I_{\text{curv}}} \right). \]  (16)

Therefore, the curvature-correcting current \( I_{\text{curv}} \) suppress the increase in the output floating reference at low- and high-temperatures.

B. Circuit for Generating Curvature-Correcting Current

The curvature-correction circuit we developed uses two curvature-correcting currents \( I_{\text{curv1}} \) and \( I_{\text{curv2}} \). We apply the current \( I_{\text{curv}} \) to node \( V_{out2} \) such that

\[
I_{\text{curv}} = \begin{cases} 
I_{\text{curv1}} & \text{(at low temp.)} \\
0 & \text{(at middle temp.)} \\
I_{\text{curv2}} & \text{(at high temp.)} 
\end{cases} \]  (17)

The architecture to generate the curvature-correcting current is shown in Fig. 4. We use a PTAT current \( I_{\text{PTAT}} \) and temperature independent currents \( I_{\text{REF1}}, I_{\text{REF2}} \) to generate the curvature-correcting current. The architecture is based on the nodal subtraction of PTAT current \( I_{\text{PTAT}} \) and the reference currents of \( I_{\text{REF1}} \) and \( I_{\text{REF2}} \). The reference currents and PTAT current are set so that \( I_{\text{REF1}} < I_{\text{REF2}} \) and that \( I_{\text{PTAT}} \) has intersecting points with both the reference currents at different temperatures \( T_1 \) and \( T_2 \) as shown in Fig. 4(a). At temperatures lower than \( T_1 \), \( I_{\text{REF1}} - I_{\text{PTAT}} \) decreases with temperature. At temperatures higher than \( T_2 \), \( I_{\text{PTAT}} - I_{\text{REF2}} \) increases with temperature. Figure 4(b) shows their subtraction currents \( I_{\text{curv1}}, I_{\text{curv2}} \). From this way, the curvature-correcting current \( I_{\text{curv}} \) is generated and applied to node \( V_{out2} \). The curvature-correcting current can be summarized as

\[
I_{\text{curv}} = \begin{cases} 
I_{\text{REF1}} - I_{\text{PTAT}} & \text{(at low temp.)} \\
0 & \text{(at middle temp.)} \\
I_{\text{PTAT}} - I_{\text{REF2}} & \text{(at high temp.)} 
\end{cases} \]  (18)

Figure 5 shows the circuit we propose for generating curvature-correcting current, which consists of a PTAT current generator, and two subcircuits that generate curvature-correcting current: one works at low temperature and the other at high temperature.

The PTAT current for the lower temperature range is less than the reference currents: \( I_{\text{PTAT}} < I_{\text{REF1}} < I_{\text{REF2}} \), and, therefore, the output transistor M_{curv1} generates subtracted current \( I_{\text{REF1}} - I_{\text{PTAT}} \). The output transistor M_{curv2} does not generate any current because transistor M_{curv2} is in the off state. The PTAT current for a middle temperature range increases more than reference current \( I_{\text{REF1}} \) and is less than reference current \( I_{\text{REF2}} \): \( I_{\text{REF1}} < I_{\text{PTAT}} < I_{\text{REF2}} \). The output transistors M_{curv1} and M_{curv2} do not generate any currents. The PTAT current for a higher temperature range increases more than the reference currents: \( I_{\text{REF1}} < I_{\text{REF2}} < I_{\text{PTAT}} \), and, therefore, the output transistor M_{curv2} generates subtracted current \( I_{\text{PTAT}} - I_{\text{REF2}} \).
C. Simulation Results

We demonstrated the curvature-correction technique by SPICE simulation. Figure 6 shows the entire circuit. The bias current of $I_{bias}$ was set to 100 nA. The reference currents $I_{REF1}$ and $I_{REF2}$ in the curvature-correction circuit were set to 160 nA and 190 nA by changing the current gain factors of the current mirror. Figure 7 shows the simulated curvature-correcting current as a function of temperature. The correcting current $I_{curv1}$ was generated at lower temperature and decreased with temperature. The correcting current $I_{curv2}$ was generated at higher temperature and increased with temperature. These correcting currents were applied to node $V_{ref2}$ through the current mirror. Figure 8 shows the output floating reference voltage. The uncorrected reference voltage is also plotted. The variations in the reference voltage were reduced to $\pm 0.3$ % from uncorrected reference variations of $\pm 2.7$ %. The maximum power consumption of the circuit was 4.6 $\mu W$ at 100 °C. The floating reference voltage circuit requires a reference current, and the reference circuit in [10] can be used for our purpose.

V. Conclusion

We developed a floating millivolt reference circuit to generate PTAT current. The circuit operation was confirmed by simulation with 0.35-µm standard CMOS parameters. The reference voltage was about 10 mV, and the variations were $\pm 2.7$ % in a temperature range from -20 to 100 °C. The curvature-correction circuit was also developed to improve the accuracy of the reference voltage. The accuracy of the reference circuit could be improved to $\pm 0.3$ % by using this correction technique. The total power consumption of the circuit was 4.6 $\mu W$ at 100 °C.

REFERENCES


