Noise-Induced Phase Synchronization among Nonidentical Analog CMOS Oscillators

Akira Utagawa†, Tetsuya Asai, Tetsuya Hirose, and Yoshihito Amemiya

Abstract

Noise-induced synchronization is a phenomenon where populations of independent oscillators are synchronized by applying common noises to the oscillators without all-to-all coupling. Recently, Nakao et al. proposed a mathematical model of the noise-induced synchronization [1]. We utilize this model for the phase synchronization of on-chip multiple clock sources in digital LSIs. We apply common noises to all the clock sources in order to synchronize the clock sources, aiming at global clock distribution without wiring delay. We report that these oscillators can be synchronized even if each clock frequency generated by several clock sources have slight difference. We constructed a Wilson-Cowan oscillator circuit with 0.25 μm CMOS parameters, which operated at 1.17 GHz. Through circuit simulations, we demonstrate that identical oscillators can be synchronized by artificial noises. Then we explore the effect of mismatches among oscillator circuits, and demonstrate that phase differences among non-identical oscillator circuits are suppressed by noises if the threshold voltage difference of a dominant MOSFET in the circuits is smaller than 12 mV.

1. Introduction

Global clock distribution systems are widely used in present digital circuits. The global clock must arrive at all the registers simultaneously to keep the operation in sequence. In practical circuits, mismatches of the arrival time of the clock called “clock skew” occur. Because the clock skew severely affects the performance of the LSIs, several technologies were proposed in recent years such as zero-skew clock distribution [2], inserting buffers to maintain skew [3], building clock distribution tree called ‘H-tree’ [4], etc.

The present solutions for the skew problems may increase both the total length of clock distribution wires and the power consumption, as well as optimization and post-processing costs. In this paper, we propose another solution for the skew problems. Nakao et al. recently reported that independent neural oscillators can be synchronized by applying common noises to the oscillators [1]. We here regard neural oscillators as independent clock sources on LSIs; i.e., clock sources are distributed on LSIs, and they are forced to synchronize with the addition of artificial (or natural if possible) noises.

2. Circuit Construction

In the original model [1], the FitzHugh-Nagumo neuron was used to demonstrate the noise-induced synchronization between the time courses of N trials under different initial conditions. Instead we use N conventional Wilson-Cowan oscillators [5] in our model that are suitable for analog CMOS implementation [6]. The dynamics are given by

\[
\begin{align*}
\tau_1 \frac{du_i}{dt} &= -u_i + f_\beta(u_i - v_i) + I(t), \\
\tau_2 \frac{dv_i}{dt} &= -v_i + f_\beta(u_i - \theta),
\end{align*}
\]

where \(u_i\) and \(v_i\) represent system variables of the \(i\)-th Wilson-Cowan oscillator, \(f_\beta(\cdot)\) the Sigmoid function with the slope factor \(\beta\), \(I(t)\) the random temporal impulse, \(\theta\) the threshold, and \(\tau_1, \tau_2\) the time constants. The random temporal impulse \(I(t)\) is given by

\[
I(t) = \alpha \sum_j \delta(t - t_j^{(1)}) - \delta(t - t_j^{(2)}),
\]

where \(\alpha\) is the strength of the impulse, \(\delta(t) = \Theta(t) - \Theta(t-w)\) (\(\Theta\) and \(w\) represent the step function and the width of the impulse), and \(t_j^{(k)}\) the arrival time of \(j\)-th impulse \((k=1, 2)\). When \(\tau_1 = \tau_2 \approx 0\) and \(I(t) = 0\), Eq. (1) can be transformed into

\[
\begin{align*}
u_i &\approx f_\beta(u_i - v_i), \\
v_i &\approx f_\beta(u_i - \theta).
\end{align*}
\]

Figure 1 shows a Wilson-Cowan oscillator circuit for sub-RF operations based on Eq. (3). The circuit consists of a differential pair (M1 to M3) and a buffer circuit composed of two standard inverters. The output voltage of OTA \((V_o)\) is expressed by \(V_{dd} \cdot f(V_1 - V_2)\), while the output voltage of the buffer circuit \((V_{o2})\) is given by \(V_{dd} \cdot f(V_{in} - V_{dd}/2)\), where
buffer circuit

Figure 1: Wilson-Cowan circuit for sub-RF operations.

![Figure 1: Wilson-Cowan circuit for sub-RF operations.](image)

\[ f(\cdot) \text{ represents a nominal Sigmoid-like function. We thus obtain} \]

\[
\begin{align*}
    u_i &= V_{dd} \cdot f(u_i - v_i), \\
    v_i &= V_{dd} \cdot f(u_i - V_{dd}/2),
\end{align*}
\]

(4)

by connecting the inputs and outputs of the OTA circuit and the buffer circuit to \( u_i \) and \( v_i \) as shown in Fig. 1 \((V_1 = V_o = u_i, V_2 = v_i, V_{in} = u_i, V_{o2} = v_i)\), which corresponds to Eq. (3).

In the Wilson-Cowan system, the noise term \( I(t) \) was added to \( u_i \)'s dynamics only. The easiest way to give noises to the proposed circuit is to couple digital M-sequence circuits with node \( u_i \) via a capacitor. The capacitor currents caused by random transitions \((0 \rightarrow 1 \text{ or } 1 \rightarrow 0)\) of the M-sequence circuits may fluctuate \( u_i \). However, since the proposed circuit is operating in the voltage mode, current injection and ejection via small capacitance may not fluctuate \( u_i \) effectively. Therefore, in the proposed circuit, the noisy term was included in the slope factor of OTA’s \( f(\cdot) \). The slope factor increases vastly as \( V_{ref} \) increases. Therefore, by fluctuating \( V_{ref} \) with \( V_{mseq} \) via \( C \), one can perturb the circuit effectively.

Figure 2: Time courses of system variables of \( i \)-th oscillator circuit receiving pseudo-random impulses.

![Figure 2: Time courses of system variables of \( i \)-th oscillator circuit receiving pseudo-random impulses.](image)

3. Simulations Results

In following simulations, we used TSMC’s 0.25-\( \mu \)m CMOS parameters with \( W/L = 0.36 \mu \text{m} / 0.24 \mu \text{m} \) except for M3’s channel length \((L = 2.4 \mu \text{m})\). Pseudo-random sequential voltage \( V_{mseq} \) was generated with a 4-bit M-sequence circuit. The clock frequency of the M-sequence circuit was set at 500 MHz, which resulted in a 30-ns pseudo-random sequence. \( C, R_o, \) and \( V_{dd} \) were set at 20 \( \Omega \), 1 \( k\Omega \), and 2.5 V, respectively. \( V_{bias} \) was set at 1 V, so that DC currents of M3 were limited up to 60 \( \mu \)A.

We conducted SPICE simulations of a single Wilson-Cowan circuit receiving \( V_{mseq} \). Figure 2 shows time courses of \( u_i \) and \( v_i \), and Fig. 3 shows nullclines and trajectory of \( u_i \) and \( v_i \). We confirmed limit-cycle oscillations where the trajectory was well fluctuated by \( V_{mseq} \). The measured oscillation frequency was 1.17 GHz.

Phase shifts of the oscillator caused by noises depend on timing of the noise arrival. The timing can be expressed by the phase of the oscillator \( \phi_i \) and the phase shift \( \Delta \phi \) is represented by a phase response curve (PRC) [7]. Figure 4 shows the simulated PRC of the proposed circuit. As shown in Fig. 4, phases of the oscillator are advanced when \( -\pi/2 \leq \phi_i \leq \pi/2 \), whereas phases are delayed when \(-\pi \leq \phi_i < -\pi/2 \) or \( \pi/2 < \phi_i \leq \pi \). Thus the phases of the oscillator converge to around \( \pi/2 \) with the appropriate strength of noises. This implies that applying common random noises to several oscillator circuits forces to synchronize their phases. Figure 5 shows the simulated raster plots (vertical bars were plotted at which \( v_i > 1.25 \text{ V} \) and \( dv_i/dt > 0 \)). All the circuits exhibited independent oscillations when random sequence \( V_{mseq} \) was not given to them.

Figure 3: Nullclines and trajectories of oscillator circuit receiving pseudo-random impulse.

![Figure 3: Nullclines and trajectories of oscillator circuit receiving pseudo-random impulse.](image)
In order to evaluate the degree of synchronization, we calculated order parameter $R(t)$. $R(t)$ is given by

$$R(t) = \frac{1}{N} \sum_j \exp(i\phi_j(t)), \quad (5)$$

where $j$ represents the oscillator number and $i$ the imaginary unit. Time courses of $R(t)$ are shown in Fig. 6. When random impulse was not given to the circuit, $R(t)$ was always less than 1 [Fig. 6(a)], while $R(t)$ approached to 1 after $t \approx 30$ ns when random impulse was given [Fig. 6(b)]. The reason why $R(t)$ did not converged to 1 is due to stiff oscillations of $v_i$; small phase differences between the oscillators were expanded at the rising and falling times of square-shaped $v_i$.

Our results indicate that if we distributed these circuits as ubiquitous clock sources on digital CMOS LSIs, they could be synchronized when common random impulses were given to the circuits. Although this may cancel out the present skew problems, device mismatches among the clock sources may prevent the sources from complete synchronization. Therefore, we investigated the device-mismatch dependence of the proposed circuits. For our distributing purposes, local mismatches in a single oscillator circuit would be negligible; i.e., mismatches in a differential pair (M1 and M2) and a current mirror. Mismatches in inverters corresponding to threshold $\theta$ in Wilson-Cowan model would also be negligible because they only shift the fixed point, and do not vastly change the oscillation frequency. However, mismatches of M3 between the oscillators may drastically change each oscillator’s intrinsic frequency. Therefore, we investigated effects of threshold voltages of M3s on synchronizing properties. Figure 7 shows time courses of phases of two oscillator circuits. As a difference of threshold voltages of two M3s ($\Delta V_{th}$) increased, the phase difference expanded. Interestingly, the phase difference of two oscillators having different intrinsic frequencies ($\Delta V_{th} \neq 0$) was almost locked when random noises were given. This is caused by simultaneous noise injection to the oscillators, and this phase-locked structure is broken when clock frequencies of the M-Sequence circuit is decreased.

Figure 8 shows dependence of maximum phase differences between two oscillators on $\Delta V_{th}$. The absolute phase differences were measured between 50 ns and 150 ns for every $\Delta V_{th}$, and we plotted the maximum phase difference. Surprisingly, when $\Delta V_{th} < 12$ mV, the maximum phase difference was fixed around $\pi/2$, which indicates that the circuit has small tolerance on device mismatches, although the phase difference exists. Using distributed oscillators as clock sources in sequential circuits with the phase difference over
\[ \pi - \pi \] (a) \( \Delta V_{th} = 0 \)
\[ \pi - \pi \] (b) \( \Delta V_{th} = 12 \text{ mV} \)
\[ \pi - \pi \] (c) \( \Delta V_{th} = 14 \text{ mV} \)

Figure 7: Time courses of phase \( \phi_i \) of two oscillators with (a) \( \Delta V_{th} = 0 \), (b) \( \Delta V_{th} = 12 \text{ mV} \), and (c) \( \Delta V_{th} = 12 \text{ mV} \)

\[ \pi - \pi \] Figure 8: Synchrony dependence on parameter mismatch.

\( \pi (\Delta V_{th} \geq 16 \text{ mV in our simulations}) \) are definitely not safe, whereas if the phase difference is smaller than \( \pi \), one can deal with this difference somehow. Still we do not have exact solutions, but our ‘ubiquitous’ clock sources with small device mismatches would be synchronized by optimizing our parameter sets. For practical implementation, we have to consider how we apply the common noises to all the oscillators. One possible solution is to use power supply noises in large-scale digital circuits. Recent power-supply noise modeling and on-chip measurement results [8] show that noises on power-supply voltages are quasi periodic, and are not negligible now. Power-supply noises on wide wires could be distributed to the clock sources without local deviation. Another idea is to use external (off-chip) electromagnetic noise sources. In this case, each clock source should implement antennas at the topmost metal layer to catch the electromagnetic noises, and other circuit block must be shielded. Our present circuit employed M-sequence circuits for the demonstration aim, they must be replaced with more practical noises that can reach at each oscillators simultaneously.

4. Conclusion

We designed CMOS sub-RF oscillators that could be synchronized using common random impulses, based on a theory in [1]. We proposed a modified Wilson-Cowan model for implementing FitzHugh-Nagumo oscillators. We then designed sub-RF oscillator circuits based on the modified Wilson-Cowan oscillator model. Through circuit simulations, we demonstrated that the circuits exhibited the synchronization properties. For our clock-distributing purposes, we investigated the synchrony dependence on device mismatches between two oscillator circuits. The result showed that i) the oscillators exhibited phase-locked oscillation and ii) the circuit had small tolerance on device mismatches, although small phase difference (\( \pi/2 \)) exists.

References