Look-Ahead Dynamic Threshold Voltage Control Scheme for Improving Write Margin of SOI-7T-SRAM

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SUMMARY Instability of SRAM memory cells derived from aggressive technology scaling has been recently one of the most significant issues. Although a 7T-SRAM cell with an area-tolerable separated read port improves read margins even at sub-1V, it unfortunately results in degradation of write margins. In order to assist the write operation, we address a new memory cell employing a look-ahead body-bias which dynamically controls the threshold voltage. Simulation results have shown improvement in both the write margins and access time without increasing the leakage power derived from the body-bias.

key words: PD-SOI, body-bias, SRAM, low power design

1. Introduction

In a previous scenario of SRAM development, technology scaling had been able to achieve the higher performance, larger memory capacity, and lower power consumption at the same time so far. However, when it comes to a sub-100nm era, an unexpected random variation in the threshold voltage \(V_{\text{th}}\) derived from the process variation and the lowered supply voltage drastically deteriorates the stability of SRAM memory cells. Then, we propose a 7T-SRAM cell adopting the active body-biasing control on PD-SOI, where the \(V_{\text{th}}\) of each transistor can be dynamically controlled through the direct body contact [1], [2]. The use of word/bit line signals as the control signals for memory cells improves both the write margins and access time.

2. Improved Write Margin by Look-Ahead Dynamic Threshold Voltage Control

In general SRAM memory cells, conflicting requirements for improving both the write and read margins have been posing significant design challenges in low voltage operation. Although the previous work such as 8T-SRAM [3] and 7T-SRAM [4] with a separated read port expands the read margins, the additional transistors result in degradation of the write margins. In addition, the write operation for 7T-SRAM using a single bit-line alone deteriorates both the write margins and access time. Even though the boosted VSS nodes in the memory cell suppress the degradation of write margins [4], it also requires additional circuits and multiple supply voltages. Then, in order to assist specially the ‘1’-write operation, we compensate the deteriorated write margins by adopting look-ahead dynamic \(V_{\text{th}}\) control on PD-SOI for 7T-SRAM cells with the improved read margins. Here, our proposed approach employs only word/bit line signals for the body-biasing control, and therefore any additional signal is not required.

2.1 SOI-7T-SRAM with Look-Ahead Body-Biasing with Word/Bit Line Signals

In the proposed 7T-SRAM cell shown in Fig. 1, the write bit line (WBL) provides the body-bias for the driver nMOS (N1) in INV(R) and the write and read word lines (WWL and RWL) control the body voltages of access nMOSs (N3, N4) and driver nMOS (N5). Here, the body voltages of pMOSs (P1, P2) and nMOS (N2) are fixed to \(V_{\text{DD}}\) and GND, respectively. In the case of ‘1’-write (write1) operation, the \(V_{\text{th}}\) of nMOS (N1) is lowered by the forward body-bias under the condition of WBL = “High”, which accelerates the discharging speed of node V2. On the other hand, during the ‘0’-write (write0) operation where the WBL = “Low”, the body voltage of nMOS (N1) is fixed to GND in the same way as the body-tied configuration, and hence the \(V_{\text{th}}\) and ‘0’-write speed remain unchanged. Namely, the \(V_{\text{th}}\) of nMOS in INV(R) can be controlled by the write data of WBL beforehand in order to assist the write operation. Moreover, the body-biases employing the WWL and RWL improve the write and read current owing to the lowered \(V_{\text{th}}\) of access nMOSs (N3, N4) and driver nMOS (N5), which
therefore shortens the access time both in write and read operation. Here, since the activated WWL would destroy the stored cell data in the unselected column in the write mode, the proposed cell should be applied with the approaches where the column is selected per written block such as the divided word line structure [5].

2.2 Layout of Memory Array with Body Contact

In order to control the body voltage of individual transistor, a body contact is required for providing the body-bias. Here, the HTI (Hybrid Trench Isolation) technology [1], [2] shown in Fig. 2 drastically reduces the area penalty and parasitic gate capacitance of the body contact to almost the same level as bulk MOSFETs. Considering the intolerable area penalty when all the body contacts are placed in each memory cell, we examine a layout style that places the body contacts in the memory cell while causing no area overhead compared to the conventional 7T-SRAM, otherwise the body contacts are shared among several memory cells aligned in the same column. Fig. 3 shows the proposed cell layout of 7T-SRAM including the body contacts for access transistors (N3, N4) and driver transistors (N2, N5). Here, the bodies of N4 and N5 are shared, and those of N2, N3, and N4/N5 are isolated from other transistors aligned in the same column. Fig. 4 illustrates the layout of memory array with the body contact cells, where the body-bias is provided to memory cells through the body contact. Here, the area overhead due to the additional shared body contacts can be reduced by increasing the number of memory cells per body contact. However, the number ($N$) of memory cells sharing one body contact has a constraint due to the relatively high resistance of the body wiring from the body contact to the body of transistor.

3. Simulation Results

We have performed SPICE simulation assuming a 90 nm process technology under the conditions that the transistor sizes are $L = 0.10 \mu m$, $W = 0.16 \mu m$ and the supply voltage is set to 0.6 V to avoid the PN leakage current passing through the body region. Regarding the device parameters of SOI MOSFETs, we have employed the BSIM4 model corresponding to bulk MOSFETs since the bodies of all the transistors can be fixed by the HTI technology [1], [2]. Here, these device parameters have been determined within the accuracy of 5% in terms of the measured oscillation period $t_{pd}$ of the ring oscillator circuit. After evaluating the write margins and access time, the leakage power due to the additional body-bias has been analyzed. Then, we have also estimated the relation between the number ($N$) of memory cells sharing one body contact and the area overhead or timing slack of the body voltage which varies due to the resistance and capacitance of body wiring. The threshold voltages are set to $V_{th-n(low)} = 0.25 V$ for the access and driver nMOSs (N1, N3) and $V_{th-n(high)}/V_{th-p(high)} = 0.39/0.44 V$ for others. We have decided the body resistances of 119 k$\Omega$, 238 k$\Omega$ for pMOS and nMOS, respectively, assuming that the body contact cell connects with the neighboring memory cells. The capacitances of word lines and bit lines for the 256 word $\times$ 32 bit memory array are also determined as $C_{WL} = 11 fF$ and $C_{BL} = 31 fF$, respectively. The proposed 7T-SRAM cell has an area overhead of 20% compared to the 6T-SRAM cell.

3.1 Evaluation of Write Margin

The ‘1’-write margins for the conventional and proposed 7T-SRAM cells are shown in Fig. 5. Here, the conventional 7T-SRAM surely fails in the ‘1’-write operation due to the serious lack of write margin. On the other hand, the voltage transfer characteristics (VTCs) for the proposed cell with the body-bias shown in Fig. 5(a) are shifted owing to the body-bias employing the look-ahead control signals of word/bit lines, which expands the write margins in the ‘1’-write modes. In addition, applying the proposed cell to the VSS-bias scheme [4], where the separated two VSS...
nodes VSSM(R) and VSSM(L) are controlled complementarily according to the data to be written, achieves the write margin of 96 mV. Here, the ‘0’-write margin remains unchanged since the $V_{th}$ of driver nMOS (N1) is never lowered owing to the WBL = “Low”.

3.2 Evaluation of Access Time

Figure 6 shows the access time in the case adopting the VSS-bias of 0.1V for the memory cell to ensure the ‘1’-write operation. The waveforms shown in Fig. 6 correspond to the clock (CLK), word lines (WWL/RWL), bit lines (WBL/RBL), data retention nodes (V1/V2), output data signal (BL$_{out}$), and body voltage ($V_{body}$). Here, the access time is defined as the period from the point of $V_{DD}/2$ in CLK during the low to high transition to that in the data retention node V2 or output data signal (BL$_{out}$) during the data inverting operation. The body-bias improves the charge and discharge current at the data nodes V1 and V2, and hence shortens the access time by 36% in the ‘1’-write and 43% in the read mode.

The write time of a 6T-SRAM cell has been calculated to be 2.84 ns by SPICE simulation in the same condition. Although the write time is degraded to 1.69x in the conventional body-tied 7T-SRAM cell, the proposed cell suppresses it to 7%. Here, a further reduction in the access time is expected by applying a proper voltage control such as the $V_{DDM}$ control and VSS-bias [6], [7].

3.3 Leakage Power Analysis

Next, we discuss the leakage power of a memory cell in the standby mode assuming at 0.6-$V_{DD}$, room temperature, and the typical process corner. In Fig. 7, although the proposed memory cell is supposed to increase the leakage power due to the body-bias, a proper control of the bit line signals avoids the exponential increase in leakage power which is actually dependent on both the bit line voltages and stored cell data. For example, the leakage power remains unchanged regardless of the stored cell data when bit lines are “Low” since the body-bias employing the WBL in the proposed cell never lowers the $V_{th}$ of driver nMOS (N1). On the other hand, when bit lines are “High” and the stored cell data is “0”, it results in the exponential increase in leakage current of driver nMOS (N1) from the node V2 due to the lowered $V_{th}$. Therefore, the leakage power derived from the body-bias in the proposed cell never increase as long as the WBL is fixed to “Low” in the standby mode.

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**Fig. 5** Improved write margins for proposed memory cell.

**Fig. 6** Access time comparison based on simulated waveforms.

**Fig. 7** Leakage power in the standby mode.
3.4 Placement of Body Contact and Timing Slack of Body Voltage

Here, we discuss the trade-off relation between the area overhead and timing slack of the body voltage for the number \(N\) of the memory cells sharing one body contact in Fig. 8. Here, the area overheads are normalized to the conventional layout style where a body contact is shared by 32 memory cells. For incorporating the extra body resistances \(R_{body}\) and capacitances \(C_{body}\) in the shared body region not included in the transistor model, we have estimated the \(R_{body}\)'s with pMOS and nMOS are 111 k\(\Omega/\mu m\) and 222 k\(\Omega/\mu m\), respectively, and \(C_{body} = 0.043 fF/\mu m\). The resistances \(R_{body}\) have been determined based on a measurement result of real devices, and the capacitance \(C_{body}\) has been calculated as the capacitance between the silicon substrate and SOI layer where the thickness \(t_{BOX}\) of buried oxide is 145 nm. Then, we have evaluated the timing slack of the body voltage at the farthest memory cell from the body contact. For the write buffer driving the body voltage and bit lines, the size is decided \(W_{buf} = 2.5 \mu m\) which is optimized in terms of the energy-delay product.

According to the results for \(N\) from 2 to 32, the timing slack \(t_{WWL} - t_{body}\) which represents the period from the \(V_{DD}/2\) in body voltage to that in WWL decreases with \(N\). In the case of memory with 256-word, even though the timing slack of the body voltage is 0.23 ns when \(N = 2\), the value is deteriorated to \(-2.82\) ns when \(N = 32\). Here, the maximum number \(N_{max}\) of sharing memory cells should be decided within the limit of controlling the body voltage perfectly before the write operation in the memory cell. The timing slack in the simulation results constrains an upper limit of \(N_{max} = 8\) which barely satisfies \(t_{WWL} - t_{body} > 0\) and hence ensure the expanded write margins before the write operation. Here, the area overhead is 10\% when \(N_{max} = 8\). Moreover, even though the ideal condition of \(t_{WWL} - t_{body} > 0\) is not satisfied, we still expect the access time reduction as long as the timing slack meets \(t_{WWL} - t_{body} > -2.53\) ns according to the write period of 2.53 ns from WWL to the data node V2 in the conventional approach shown in Fig. 6(a).

4. Conclusion

In order to improve the deteriorated write margin of a 7T-SRAM cell, we have proposed a memory cell adopting a look-ahead body-bias which dynamically controls the threshold voltage in order to assist the write operation. Simulation results have shown improvement in both the write margins and access time without increasing the leakage power derived from the body-bias.

References


