A Technique for High-Speed Circuits on SOI Using Look-Ahead Type Active Body Bias Control

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1. Background

Designing LSI ...

Scaling down

Transistor: 130 nm 90 nm 65 nm

getting difficult to maintain Scaling Principle ...

because of "Power Dissipation"

Dynamic Power: becoming lower per Gate by scaling down
Leakage Power: becoming larger even per Gate + Integration
-> awfully increasing

In the future, Dynamic Power ≪ Leakage Power estimated

"Leakage Power Reduction" is significant problem !!
LSI will be no longer depends on only scaling down in the future!!

**SOI Transistor** attracts attention

**Feature of SOI (Silicon On Insulator) is …**

- Lower junction capacity
- High-speed, Low power
- Body Terminal

SOI’s merits:
- Lower junction capacity
- High-speed, Low power
- Body Terminal
- Vth could be controllable

ABB: Active Body Bias

†† PD: Partially Depleted

Bulk MOSFET

SOI MOSFET (PD† SOI)
Example of Vth Control

DTMOS (Dynamic Threshold voltage MOS)

Gate signal connects to Body

→ Lowering \( V_{th} \) while switching  

\[ \text{speed up} \]

\[ \begin{align*} 
\text{in} = \text{Low} : & \quad \text{pMOS Low-} \ V_{th} \\
\text{in} = \text{High} : & \quad \text{nMOS Low-} \ V_{th} 
\end{align*} \]

DTMOS

Restriction in DTMOS

When \( V_{n-body} \geq 0.6 \text{ V} \)

nMOS

\[ \text{VDD must be less than 0.6 V}!! \]

Gate

Drain

Source

PN Current
1. Background

**ABB method with subsidiary transistor**

DTMOS inverter with sub transistor

Vref-p

Vref-n

in

out

\[ V_{n-body} \leq 0.6 \text{ V} \]

Adjusting \( V_{ref-n}, V_{ref-p} \)

Suppress PN Current

No restriction on \( V_{DD} \) !!

But …

*one problem still remains in conventional ABB method.*
2. Our Goal

2 ideas for “LA-ABB” to achieve High-speed & Low-leakage

(1) Focus on differences in arrival time of input signals
   - Apply to “Manchester Carry Chain Adder”

(2) Use signals generated from previous stage
   - Apply to “High-speed 16:1 MUX”

Control body voltage earlier only if needed

Waiting in Low $V_{th}$ status

Shorten delay time without leakage increase
Problem of conventional ABB method

DTMOS inverter with sub transistor actually causes longer delay than usual inverter!!

Because of …

- Still **High-$$V_{th}$$** at the moment turning ON.
- Less effective for high-speed circuits due to delay with body voltage.

- Already **Low-$$V_{th}$$** before Gate signal rises.
- Preceding signal is able to lower $$V_{th}$$ beforehand.

Conventional ABB

LA-ABB

**“Preceding signal”**

**“Controlling $$V_{th}$$ beforehand”**
3. LA-ABB and Its application

LA-ABB method

What’s the condition to control $V_{th}$ beforehand??

(1) Gate signal arrives earlier than Source signal
(2) Control body voltage by some signal except Gate

Make use of 2 conditions to lower $V_{th}$ beforehand
3.1 Application to Manchester Carry Chain Adder

LA-ABB method

(1) Gate signal arrives earlier than Source signal

4bit Manchester Carry Chain Adder

Aims at high-speed carry signal propagation
3.1 Application to Manchester Carry Chain Adder

Algorithm to calculate Carry out

Input: \( a_i, b_i, C_i \)
Output: \( C_{i+1} \) (carry out)

\[
\begin{align*}
\begin{array}{c|c|c|c}
\text{carry kill} & \text{carry propagation} & \text{carry generation} \\
\hline
0 & 0 & \text{Carry kill } k_i = 1 \\
0 & 1 & \text{Carry propagation } p_i = 1 \\
1 & 0 & \text{ } \\
1 & 1 & \text{Carry generation } g_i = 1 \\
\end{array}
\end{align*}
\]

Utilize this algorithm of calculation !!

\[
\begin{align*}
\begin{cases}
  k_i = a_i \cdot \overline{b}_i \\
p_i = a_i \oplus b_i \\
g_i = a_i \cdot b_i
\end{cases}
\Rightarrow C_{i+1} = \overline{k_i} (g_i + C_i \cdot p_i)
\end{align*}
\]
4bit Manchester Carry Chain Adder’s critical path

When carry signal propagates from C0 to C4 delay time must be longest.

: applying LA-ABB to transfer gates.
Each transfer gate is in the state of waiting for carry signal.

“Lowering $V_{th}$” affects speed-up propagation.

LA-ABB technique for speed-up

3.1 Application to Manchester Carry Chain Adder
3.2 Application to 16:1 MUX Circuit

**LA-ABB method**

(2) Control body voltage by some signal except Gate

- LA-ABB for D-FF
- LA-ABB for inverter

Control $V_{th}$ by preceding signal → Speed-up

$V_{ref-p}$: High $V_{th}$

$V_{ref-n}$: Low $V_{th}$
3.2 Application to 16:1 MUX Circuit

Critical section in 16:1 MUX circuit

4:1-MUX

4:1 Selector

Control signal generator

1/4 divider

4 bit Data

Data OUT

clock

4:1-MUX

S1 S2 S3 S4

D1 D2 D3 D4

D1B D2B D3B D4B

SOUT SOUTB

LA-ABB for D-FF, inverter

are applied only to 4:1 MUX circuit in order to suppress extra power caused by sub transistor.
4. Experimental Results

Simulation conditions

- Process rule: 0.18 μm PD-SOI
- RC on wire:
  - Manchester Carry Chain: extract RC from Layout
  - 16:1MUX Circuit: assign 20 ~ 80 fF

Comparison among these techniques

- Circuit simulation by HSPICE evaluated
  - Delay
  - Power dissipation
  - Leakage current

Cell Layout

Assigning Low-$V_{th}$ only to critical path.
Others: High-$V_{th}$. 

Gate

Source

Drain

Body-tie (conventional)

LA-ABB

Dual $V_{th}$
4.1 Result with Manchester Carry Chain Adder

- Delay [ps]
  - Body-tie (conventional)
  - Dual Vth
  - LA-ABB (Proposed)

- Power [µW]

LA-ABB:

- **Speed**: 20% improvement compared to Body-tie.
- **As fast as Dual Vth.**
- **Power**: 3% degradation because of sub-Tr.
4.1 Result with Manchester Carry Chain Adder

Comparison in Standby mode

Leakage current [nA]

- Body-tie (conventional)
- Dual Vth
- LA-ABB (Proposed)

Dual Vth: 16x of leakage with Body-tie, LA-ABB.

LA-ABB: saving standby power as well as Body-tie.

In comparison with Dual Vth, LA-ABB is much more effective for high-speed technique without degradation in leakage.
### 4.2 Result with MUX Circuit

#### Max frequency in MUX circuit [GHz]

- **Body-tie (conventional)**
- **Dual Vth**
- **LA-ABB (Proposed)**

#### Power [mW] @Active

- VDD = 1.2 V, 29.3 mW
- VDD = 1.5 V, 31 mW
- VDD = 1.8 V, 29.6 mW

#### Leakage current [mA] @Standby

- VDD = 1.2 V, 1.93 mA
- VDD = 1.5 V, 3.11 mA
- VDD = 1.8 V, 63.4 mA

**LA-ABB:**

- 5% improvement compared to Body-tie

**VDD:** 1.2 V

**Clock:** 4 GHz

5% improvement compared to Body-tie
5. Summary

Feature of SOI: Dynamic $V_{th}$ Control

**LA-ABB method**

- **idea 1** Gate signal arrives earlier than Source signal
  - 20% speed-up on Manchester Carry Chain Adder.

- **idea 2** Control body voltage by some signal except Gate (LA-ABB for D-FF, inverter)
  - 5% max. frequency improvement on 16:1MUX.

LA-ABB is more suitable for leakage reduction than Dual $V_{th}$.

<table>
<thead>
<tr>
<th>item</th>
<th>Body-tie</th>
<th>Dual $V_{th}$</th>
<th>LA-ABB</th>
</tr>
</thead>
<tbody>
<tr>
<td>speed</td>
<td>△</td>
<td>O</td>
<td>O</td>
</tr>
<tr>
<td>leakage</td>
<td>O</td>
<td>X</td>
<td>O</td>
</tr>
</tbody>
</table>

Future work

Leakage power reduction with SOI in ultra low $V_{DD}$