Active Body-Biasing Control Technique for Bootstrap Pass-Transistor Logic on PD-SOI at 0.5V-VDD

M. Iijima, M. Kitamura, K. Hamada, K. Fukuoka, M. Numa, A. Tada†, and S. Maegawa†
Kobe University, 1-1 Rokko-dai, Nada, Kobe 657-8501, Japan
†Renesas Technology, 4-1 Mizuhara, Itami, Hyogo 664-0005, Japan
numa@kobe-u.ac.jp, +81(78) 803-6089
†maegawa.shigeto@renesas.com, +81(72) 784-7324

Abstract
In this paper, we propose an Active Body-biasing Controlled (ABC)-Bootstrap PTL (Pass-Transistor Logic) on PD-SOI at 0.5 V-VDD for ultra low power design. Applying active body-biasing to Bootstrap PTL is the key for higher performance without output voltage loss by boosting gate voltage with coupling capacitance between source and body. Lowering $V_{th}$ by body biasing also contributes for high speed operation. Experimental results have shown improvement in both delay time and power consumption.

Introduction
Aggressively scaled-down CMOS technology faces the speed-improvement degradation due to increase in power consumption. Lowering threshold voltage causes the drastic increase in leakage power. The low power design style is moving from coarse-grained approaches to fine-grained ones for ultra low power operation [1].

SOI MOSFET has been attracting attention as a new device technology for improvement in both speed and power consumption in recent years [2]. In addition, PD-SOI is able to control the threshold voltage ($V_{th}$) by changing body voltage. Although VTCMOS (Variable Threshold CMOS) [3], well known as one of dynamic $V_{th}$ control techniques, controls $V_{th}$ at block level, PD-SOI is suitable for the control of $V_{th}$ at transistor level because the body region of transistor is separated each other [4]. DTMOS (Dynamic Threshold MOS) [5], also known as ABC (Active Body-biasing Control) technique, enables transistors to turn on quickly without increase in leakage power by lowering $V_{th}$ only if needed. However, DTMOS cannot be used with supply voltage ($V_{DD}$) over 0.6 V due to PN current from source / drain to substrate.

In order to achieve ultra low power operation, lowering supply voltage has been one of the most effective approaches since dynamic power consumption decreases in proportion to the square of $V_{DD}$. Lowering $V_{DD}$, however, causes degradation in performance seriously. Thus we employ the dynamic body control technique at 0.5 V-$V_{DD}$. Scaling $V_{DD}$ down to 0.5 V enables the application of ABC-technique in SOI circuits without any additional circuits for voltage level conversion.

ABC-Bootstrap PTL
The Pass-Transistor Logic (PTL), such as LEAP (LEAn integration with Pass-transistors) [6], is suitable for low power design because PTL circuit is synthesized with fewer number of transistors than CMOS logic. In addition, the low parasitic junction capacitance with SOI devices between silicon substrate and source / drain is effective to speed up PTL circuits composed of plural nMOSFET’s connected in series. The single-rail type PTL, however, has the disadvantage of voltage loss at the high-level output. Even though the output voltage $V_o$ is expected to be $V_o = V_{DD}$, the output voltage is actually able to rise only up to $V_o = (V_{DD} - V_{th})$, which causes increase in short circuit current and degradation of driving power.

The use of Bootstrap PTL [7] has been discussed to overcome the issue of output voltage loss and degradation of speed. The key point with Bootstrap PTL is that the drain voltage of nMOS pass-transistor is able to rise up to $V_{DD}$ without using pull-up pMOS by boosting the gate voltage higher than $V_{DD}$. A Bootstrap PTL configuration consists of two nMOS’s T1 and T2 as shown in Fig. 1 (a). nMOS T1 is a pass-transistor for

![Fig. 1: Bootstrap PTL.](image)

![Fig. 2: Boosting effect of Gate voltage.](image)
data propagation and T2, called “isolation transistor,” ensures capacitive coupling in T1 between source and gate, so that the gate voltage of T1 rises up higher than $V_{DD}$. The capacitance $C_{GS}$ between source and gate helps to boost gate voltage when the source signal begins to rise as shown in Fig. 2.

We propose ABC-Bootstrap PTL shown in Fig. 1 (b) to improve speed and driving power with conventional Bootstrap PTL by the following two points:

i) Speed-up by forward body-biasing higher than $V_{DD}$. This is effective to lower $V_{th}$ than conventional Bootstrap PTL. In contrast to the conventional approaches using multiple-supply voltages for forward body-biasing, single-$V_{DD}$ is enough to do so by ABC-Bootstrap PTL. Moreover, ABC-Bootstrap PTL offers improvement in boosting effect of gate voltage as shown in Fig. 2. Only the coupling capacitance $C_{GS}$ between source and gate is used to boost the gate voltage in conventional Bootstrap PTL. On the other hand, the coupling capacitance $C_{S-body}$ between source and body is also used to boost the gate voltage in ABC-Bootstrap PTL. This is the key idea with our technique to improve both speed and driving power.

Simulation Results

We have performed SPICE simulation with BSIM3-based SOI transistor model. The process rule is 0.18 μm PD-SOI and the supply voltage is 0.5 V. The threshold voltages with nMOS and pMOS are set to $V_{th,n} = 0.24$ V, $V_{th,p} = -0.34$ V, respectively. ABC-Bootstrap PTL has been applied to XOR gate [7] and to 4-bit MCC Adder [8].

In Fig. 3 shows the trade-offs between delay and standby leakage power when $V_{th}$ changes from 240 mV to 310 mV at 10 mV step. In terms of delay time, ABC-Bootstrap PTL shows the better result with speed degradation caused by higher $V_{th}$. In case of conventional Bootstrap PTL, delay time increases rapidly for higher $V_{th}$. The delay time with conventional Bootstrap PTL is 3.3 times as long as that of nMOS-only PTL when $V_{th}$ is 310 mV. Therefore, ABC-Bootstrap PTL shortens delay time effectively and avoids the speed degradation caused by high $V_{th}$. Each circuit dissipated almost the same standby leakage power as long as $V_{th}$ is kept unchanged. ABC-SOI contributes to speed up without increasing standby leakage power because ABC-SOI operates like body-tied SOI at standby mode.

We have compared the power consumption of XOR gate, 4-bit MCC Adder after adjusting proper supply voltages in order to achieve same operation speed. As shown in Table 1, both active power and standby leakage power have been decreased effectively. ABC-Bootstrap PTL saves active power by 21%, 40% for XOR gate, 4-bit MCC Adder, respectively. Moreover, the standby leakage power is also reduced by 19%, 37%, respectively.

Conclusion

We have proposed ABC (Active Body-biasing Controlled) -Bootstrap PTL with PD-SOI for high-speed operation even at 0.5 V-$V_{DD}$. One of the advantages is speed-up by forward body-biasing higher than $V_{DD}$, and the other is making use of the coupling capacitance $C_{S-body}$ between source and body to boost gate voltage higher than conventional Bootstrap PTL. As a result, our technique has succeeded in the operation of no less than 4 pass-transistors connected in series at 0.5V-$V_{DD}$.

References


Table 1: Power saving effect by ABC-Bootstrap PTL

<table>
<thead>
<tr>
<th>circuit</th>
<th>$V_{DD}$</th>
<th>Delay [ns]</th>
<th>Active Power [nW]</th>
<th>Standby Power [nW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>XOR</td>
<td>conv.</td>
<td>0.56 V</td>
<td>1.54</td>
<td>28.4</td>
</tr>
<tr>
<td></td>
<td>proposed</td>
<td>0.50 V</td>
<td></td>
<td>22.5 (0.79)</td>
</tr>
<tr>
<td>4bit-MCC Adder</td>
<td>conv.</td>
<td>0.63 V</td>
<td>9.02</td>
<td>447</td>
</tr>
<tr>
<td></td>
<td>proposed</td>
<td>0.50 V</td>
<td></td>
<td>266 (0.60)</td>
</tr>
</tbody>
</table>

Fig. 3: Variation of delay and standby power for several $V_{th}$.