Active Body-Biasing Control Technique for Bootstrap Pass-Transistor Logic on PD-SOI at 0.5V-VDD

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5. Summary

*ABC: Active Body-biasing Control
**PTL: Pass-Transistor Logic
1. Background and Goal

Power crisis due to aggressive scaling down!!

SOI (Silicon On Insulator)

*Merit* : high-speed, low power,

**ABC (Active Body-biasing Control)**

\[
\text{Power} = \rho_t \cdot f \cdot C_L \cdot V_{DD}^2
\]

- Available for transistor level.
- Speed-up without increase in standby leakage power.
- Effective for low supply voltage (no additional circuit @VDD = 0.5 V)

Hybrid Trench Isolation

SOI MOSFET
1. Background and Goal

PTL (Pass-Transistor Logic)

Merits:  - Synthesized with fewer transistors than CMOS logic.
         - Brings advantage of low junction capacitance with SOI.

PTL’s issue: voltage loss

\[ V_{drn} = V_{DD} - V_{th} \]

even when drain is “High”.

Speed degradation, lack of driving power

Bootstrap PTL

- Using capacitive coupling between Source and Gate.
- Overcoming voltage loss issue by boosting \( V_G \) higher than \( V_{DD} \).

Our goal

Low power technique for 0.5V-\( V_{DD} \)
using Active Body-Biasing Control with PD-SOI

Voltage loss becomes serious as \( V_{DD} \) goes down!!}

No use in boosting when connected in series!!
Advantage of ABC-Bootstrap PTL:

- Forward body bias higher than $V_{DD}$.
- Boosting gate voltage by capacitive coupling between source and body ($C_{S\text{-body}}$).

1: Reduction of voltage loss with $V_G$ during Low to High transition.
2: Capacitive coupling with $C_{S\text{-body}}$ also boosts gate voltage ($V_G$).

Improves speed and driving power.
2. Low Power Technique by ABC-Bootstrap PTL

Gate voltage variation for Tr. sizing

Large Tr. size brings strong boosting effect to $V_{\text{gate}}$ owing to large coupling capacitance.

Ex. $V_{\text{gate}} = 530 \text{ mV} @ W = 1.0 \mu m$
$V_{\text{gate}} = 620 \text{ mV} @ W = 2.0 \mu m$

Shorten transition time of $V_{\text{drn}}$.
3. Application to Arithmetic Circuits

Application 1: XOR gate

- No cell area penalty compared to conventional Bootstrap PTL.
- nMOS PTL and ABC-nMOS PTL are selected for comparison.
3. Application to Arithmetic Circuits

Application 2: MCC (Manchester Carry Chain) Adder

ABC-Bootstrap PTL for 4bit-MCC (proposed)

- Gate signal arrives before source signal comes.

Gate voltage is boosted beforehand.
3. Application to Arithmetic Circuits

Cell layout of 4-bit Adder with ABC-SOI
4. Circuit Simulation and Discussion

Simulation setup for HSPICE

- Process: 0.18 \( \mu \text{m PD-SOI} \)
- Supply voltage: 0.5 V
- Threshold voltage: \( V_{th-n} = 0.24 \text{ V} \), \( V_{th-p} = -0.34 \text{ V} \)
- Transistor size
  - Pass-Tr.: \( W = 2 \mu \text{m} \)
  - Isolation Tr.: \( W = 0.5 \mu \text{m} \)

Result for XOR gate

- 75\% speed-up by ABC-Bootstrap PTL.
- Almost no increase in power consumption.
  (Reduction of short circuit power in spite of consuming extra body-charging power.)
4. Circuit Simulation and Discussion

**Result for XOR gate**

![Trade-off between delay and standby leakage power](image)

- Although conventional Bootstrap PTL suffers from speed degradation as Vth goes high, ABC-Bootstrap PTL relaxes the problem.
- Almost same standby power as long as Vth is kept unchanged.
4. Circuit Simulation and Discussion

Result for 4bit-MCC Adder

Point: variation of gate and drain voltage when pass-Transistors are connected in series.

- **Short transition time at 1st stage pass-Tr.**
- **Useless gate signal due to lack of driving power causes much longer transition time.**

![Graphs showing voltage changes over time](image)
4. Circuit Simulation and Discussion

Power saving effect by ABC-Bootstrap PTL

How much can we save power when operating at same speed?
(Conventional Bootstrap PTL vs. ABC-Bootstrap PTL)

Power saving effect

Active power
XOR: \( V_{DD} = 0.56 \text{V} @\text{conv.} \)
MCC Adder: \( V_{DD} = 0.63 \text{V} @\text{conv.} \)

Standby power
XOR: \( V_{DD} = 0.50 \text{V} @\text{proposed} \)
MCC Adder: \( V_{DD} = 0.50 \text{V} @\text{proposed} \)

Applying ABC-Bootstrap PTL offers...
Active power **40%**, Standby power **37%** down
5. Summary

Low power technique for 0.5V-$V_{DD}$ utilizing

- PD-SOI’s Active Body-Biasing Control
- Bootstrap Pass-Transistor Logic (aims at avoiding speed degradation due to lowering VDD)

**ABC-Bootstrap PTL**

- Forward body bias higher than $V_{DD}$
- Boosting gate voltage by capacitive coupling.

Spice simulation results:

- **75%** speed improvement compared to conventional approach in XOR gate.
- 4-bit adder with ABC-Bootstrap PTL saves **40%** of active power as long as operating at same speed.

Future work: - Evaluation of signal integrity (noise immunity)